Date of Webinar: 1/9/18

The Design Engineer: Weak link or Warrior in the ESD Battle?

Abstract:

Design Engineers strive to incorporate ESD protection into chip designs, but they are often unclear about the best way to handle the physical devices. The Industry Council on ESD Targets documented a need to lower both the HBM and CDM thresholds with the confidence that factories already had the appropriate ESD control programs in place. However, many engineering labs do not understand or follow industry ESD guidelines and are unaware of the potential jeopardy created by these lower thresholds. Anyone doing device testing, characterization, TLP stress testing, board level analysis or upgrading their own computer should know basic ESD control techniques.

This seminar will include practical ESD control tips for engineering labs as well as how to set up and monitor a comprehensive ESD control program. Real world examples will show the increased ESD risk of Charged Board Events (CBE), the surprising damage due to hand tools and how to use event detectors to identify ESD threats.

You've spent a lot of effort doing careful designs – now take good care of your valuable test chips and prototype engineering samples.